INTEGRATION OF A 200V, 60 MHz LATERAL PNP TRANSISTOR WITH EMITTER-BASE SELF-ALIGNED TO POLYSILICON, INTO A HIGH VOLTAGE BICMOS PROCESS

Pour le titre du livre voir en seconde page

Michael P. Masquelier and David N. Okada

Semiconductor Research and Development Laboratory
Motorola, Inc., Phoenix, AZ 85008

ABSTRACT

A lateral PNP with emitter and base self-aligned to a polysilicon field plate, is designed utilizing the existing layers of a high voltage LOCOS BiCMOS process. The NHV implant is self-aligned to polysilicon, forming both the LDD NMOS and the N-base of the improved lateral PNP. The standard PMOS source-drain implant also forms the P^+ emitter diffusion and the collector contact of the improved lateral PNP. The laterally graded N-base impurity concentration provides a horizontal drift electric field, and the double-diffused technique allows a narrow base width. The polysilicon field plate, to which the emitter and base are self-aligned, is electrically biased to the emitter potential, preventing surface inversion of the base. A f_τ value of 60 MHz is obtained for the integrated lateral PNP device using s-parameter extraction. This compares to a typical value of about 1.5 MHz for a conventional structure.

The P^- CMOS field implant forms an extended collector, which accomodates the depletion region spread associated with large collector-emitter bias, and reduces the surface electric field avoiding premature breakdown. The doping level, junction depth, and drawn length of the P^- collector extension determines the maximum operating voltage of the device but also affects the collector resistance. Devices were designed, fabricated, and electrically characterized. The saturation region resistance for a conventional device with the same breakdown voltage is nearly three times that of the improved device; and the latter does not exhibit a 'quasi-saturation' region, which can cause additional power dissipation during switching.

INTRODUCTION

In lateral PNP bipolar transistor design, there exists a tradeoff between current gain (ß) or switching speed, and breakdown voltage, BV_{CEO}. Analog circuit designers have expressed the need for a high voltage lateral PNP to complement the performance of the standard NPN transistor. For a conventional lateral PNP device in which both the emitter and collector diffusions occur at the same processing step, increasing the base width to accommodate more voltage will obviously decrease the speed and ß of the device.

Several techniques have been implemented to improve the characteristics of the lateral PNP. Addition of a deep, graded P-type diffusion into the already existing shallow, heavily-doped collector will provide an increase in Early voltage [1]. This allows more of the collector-emitter voltage to be absorbed by the collector side of the collector-base junction, thereby lessening the extent of depletion region spread into the base. If the existing collector junction is curvature-limited, this technique can also provide an increase in breakdown voltage. If the P-well is used to provide this additional diffusion, it can be difficult to attain the self-alignment necessary to control base width, since the deeper P-well must be formed much earlier in the process.

A second technique which allows a smaller base width for a given breakdown voltage, involves surrounding the emitter with a N-layer which is more heavily doped than the existing base region [2]. This emitter punchthrough shield prevents the collector-base depletion region from reaching the emitter. Under normal operating conditions, the collector-base depletion boundary reaches the punch-through shield. The resultant smaller base width reduces minority carrier base transit time, increasing device switching speed. The higher base Gummel number of this structure also reduces base width modulation. Both of these ideas have been incorporated into a single device in which the emitter and base implants are self-aligned to an oxide step [3]. A lightly doped P^- collector provides high BV_{CEO}, while the narrow graded base allows fast switching.

The improved lateral PNP device presented here incorporates a polysilicon field plate which simultaneously provides self-alignment of the emitter and base implants, and distribution of surface electric fields in the base and extended collector regions [4]. This device has been integrated into a high-voltage BiCMOS process.

PROCESS INTEGRATION

The devices are fabricated utilizing the existing diffusions of a high voltage BiCMOS process which employs junction isolation to separate the CMOS and bipolar circuitry from the lateral DMOS or Up-drain DMOS power output device. A cross-section of the previously existing devices from this process are displayed in Figure 1. An Antimony spin-on is used to form the N^+ buried layer in a P substrate. An N epitaxial layer (18 µm, 8 Ω-cm) is grown, followed by a deep P^+ isolation diffusion. The N^+ sinker is formed by PH_3 predeposition and diffusion, providing the drain current path for the up-drain DMOS, as well as the base current path for the improved lateral PNP, as shown in Figure 2. The P-well is formed to fabricate the NMOS devices, as well as provide the junction termination to increase the P^+ to N epitaxy breakdown for the collector of the improved lateral PNP. The CMOS devices are locally isolated with standard LOCOS, and a P^- field implant is used to prevent surface channels, as well as form the extended collector for the improved lateral PNP. After formation of a 600Å gate oxide, a 3500Å polysilicon deposition and patterning, the PHV implant forms the lateral DMOS channel and can be used to form a graded drain for a high voltage PMOS. The NHV implant which is used to fabricate high voltage NMOS and self-aligned to polysilicon to form the base of the improved lateral PNP. The standard PMOS source-drain implant also forms the P^+ emitter diffusion and collector contact of the improved lateral PNP.

Figure 3 shows the vertical impurity profile through the base and emitter, measured with a spreading resistance probe. The NHV implant dose is 3.0×10^{13} cm^{-2} and the P^+ implant dose is 4.0×10^{14} cm^{-2} for this profile.

DEVICE DESIGN AND SIMULATION

In the improved lateral PNP the P^+ emitter and N-base diffusions are self-aligned. This provides a mean of fabricating a high voltage lateral PNP with a controllable, narrow base width. A P^+ emitter junction depth of 0.4 µm and a N-base junction depth of 3.6 µm yields a lateral base width of approximately 2.5 µm. The lateral N-base impurity concentration profile is graded, providing a horizontal drift electric field, enhancing both ß and f_τ. To achieve a large BV_{CEO}, the lightly doped P^- region forms an extended collector which serves to accommodate the depletion region spread and reduces the surface electric field avoiding premature breakdown. The collector-base polysilicon field plate which is used for collector to N-epitaxy

CH2987-6/91/0000-0056 $1.00 ©1991 IEEE

91CH2987-

Proceedings of the

3rd International Symposium on Power Semiconductor Devices and ICs

Edited by

M. Ayman Shibib
AT&T Bell Laboratories

B. Jayant Baliga
North Carolina State University

Sponsored by:
IEEE Electron Devices Society
Co-Sponsored by:
IEE of Japan

3rd International Symposium on Power Semiconductor Devices and ICs

ISPSD '91

Stouffer Harborplace Hotel, Baltimore, Maryland, USA April 22-24

IEEE

junction termination is electrically biased at the collector potential. The polysilicon field plate for emitter and base self-alignment is electrically connected to the emitter potential, preventing inversion of the N-base region. The concentration of the P^- collector region is chosen such that under high operating voltage, the depletion region spreads mostly into the collector and not into the base region. This tends to reduce basewidth modulation effects (increases Early voltage) and provides a high BV_{CEO} (by avoiding punchthrough), even though a narrow base exists.

Since this P^- region must collect holes injected across the base region at all operating voltages, the doping level and depth of this layer determines the maximum operating voltage of the device and affects the collector resistance.

Numerical device simulations were performed to investigate the effect of the collector extension doping profile on the electric field distributions and depletion region boundaries of the collector-base junction. Simulated impurity concentration profiles obtained using SUPREM-3 [5], were transferred into the 2-D single carrier Poisson's equation solver, CANDE [6], to obtain depletion region spreads, equipotential contours, and breakdown voltages. The graphical output of a typical simulation shown in Figure 4 reveals equipotential contours in 25V increments for an emitter to collector bias of 200V, and the depletion region boundaries.

Figure 5 demonstrates the 2-D simulations used to analyze base punchthrough. Figure 5a shows an enlarged view of the punchthrough condition in the emitter base region with a base surface concentration of 2.0×10^{17} cm^{-3}, an emitter bias of 200V and the collector grounded. Figure 5b displays the depletion region boundaries when increasing the base surface concentration to 1.0×10^{18} cm^{-3}, with the same bias voltage. The emitter-base depletion region has not merged with the collector-base depletion region, illustrating the elimination of base punchthrough.

RESULTS AND DISCUSSION

A set of lateral PNP devices were fabricated with the extended collector length varying from 12 µm to 28 µm. Figure 6 is a die photo of the lateral PNP with a 28 µm drawn collector extension. The drawn emitter diameter is 9 µm.

DC Electrical Characterization

Figure 7 shows a curve tracer I-V photo of the improved lateral PNP demonstrating a BV_{CEO} of approximately 200 volts. The typical current gain for this non-optimized device is approximately 10. Improvement to the current gain can be achieved by increasing the doping concentration of the P^+ emitter, since this device is emitter injection limited. Figure 8 illustrates the expected trend of a decrease in BV_{CEO} with a decrease in N-base implant dose. A decrease in the amount of majority carrier charge in the base allows the depletion region from the collector-base junction to spread through the base and reach the emitter at a bias of 25V with a N-base dose of 1.0×10^{13} cm^{-2}. The curves for the 20 µm extended collector device and the 28 µm extended collector device are virtually identical, indicating that the collector-base depletion region does not extend beyond 20 µm into the extended collector, before base punchthrough occurs. The reduction in BV_{CEO} as the collector extension length is decreased from 20 µm to 12 µm, results from the depletion region spread into the P- field region reaching the P+ collector contact. After this occurs, further increase of collector voltage substantially increases the electric field intensity within the depletion region resulting in avalanche breakdown of the collector-base junction.

Figure 9 compares the typical saturation region curves of a conventional 200 volt BV_{CEO} lateral PNP transistor to the improved lateral PNP with the same breakdown voltage. The conventional structure incorporates a P-well diffusion placed around the collector contact, and a 24 µm base width. The resistance in the saturation region for the conventional device is nearly three times that for the improved device. In addition, the improved device does not exhibit a 'quasi-saturation' region, which can cause additional power dissipation during switching.

The operating voltage of the collector-base junction determines the extent of the depletion region spread into the extended collector of the P^- field region. The portion of this region which is not depleted of mobile carriers contributes to the resistance between the emitter and collector. Figure 10 indicates the increase in measured saturation voltage, $V_{CE(sat)}$, with increased extended collector length. Saturation voltage, which is defined in this case for $I_C = 1.0$ mA and $I_B = 400$ µA, is shown to have a dependence of 10 mV/µm of extended collector.

AC Electrical Characterization

The unity-gain frequency (f_T) was derived from TECAP [7] s-parameter extraction. As revealed in Figure 11, a $f_{T\,(max)}$ value of 60 MHz was obtained for the improved lateral PNP device . This compares to a typical value of about 1.5 MHz for the conventional structure to which this has been compared.

CONCLUSION

A 200V BV_{CEO} lateral PNP transistor with improved frequency response over conventional designs has been designed and fabricated, utilizing only the existing layers of a BiCMOS process suitable for power integrated circuits. The self-alignment of the emitter and base implants to the edge of a polysilicon field plate, provides a narrow, graded base region with a very repeatable base width. The 2.5 µm base width provides a f_T value that is 40 times larger than that of conventional lateral PNPs with the same BV_{CEO}. During layout the extended collector length is drawn only as long as is necessary to achieve the required breakdown voltage, resulting in a significant area savings, minimal collector resistance, and reduced power dissipation.

REFERENCES:

[1] S. Krishna and A. Ramde, "A Simple Technique for Improving Lateral PNP Transistor Performance," *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 781-783, 1982.

[2] J. D. Beasom, "A High Performance High Voltage Lateral PNP Structure," in *IEDM Tech. Dig.*, 1983, p. 424.

[3] Y. Sugawara and T. Kamei, "A High-Performance High-Voltage Self-Aligned Double-Diffused Lateral (SADDL) p-n-p Transistor," *IEEE Trans. Electron Devices*, vol. ED-33, p. 23, 1986.

[4] M.P. Masquelier, "A 200V, 60 MHz Lateral PNP Transistor with Polysilicon Self-Aligned Emitter-Base, and Extended Collector," M.S.E.E. Thesis, Department of Electrical and Computer Engineering, Arizona State University, Tempe, Arizona, December 1989.

[5] SUPREM-3 One-Dimensional Process Analysis Program, Technology Modeling Associates, Version 3-3, 1986.

[6] CANDE Two-Dimensional Device Analysis Program, Technology Modeling Associates, Version 2-2, 1986.

[7] Hewlett-Packard 94445A TECAP User's Manual, 1987.

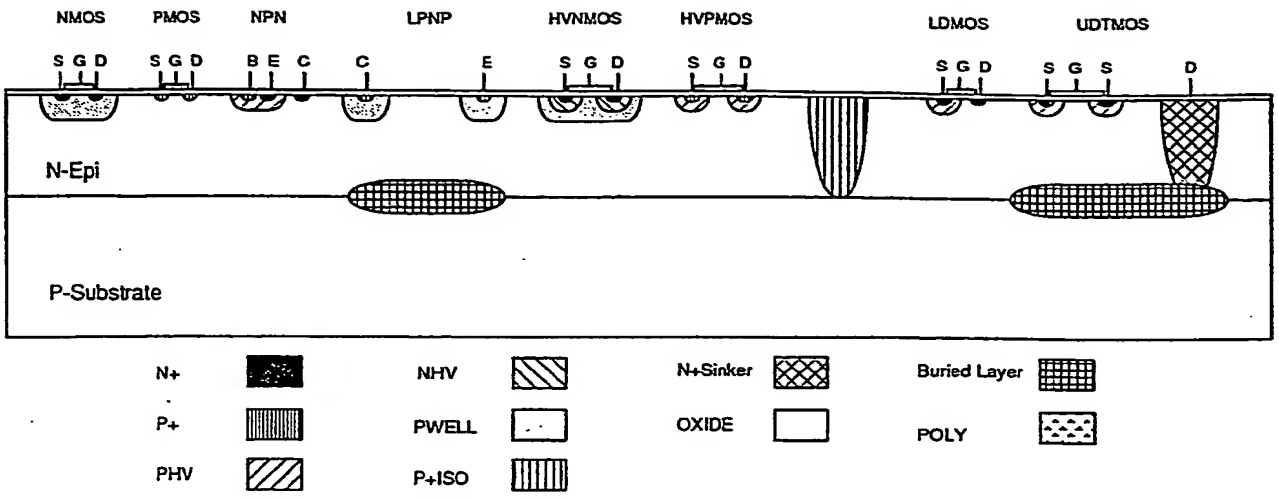


Fig. 1 Existing device cross-sections of the high-voltage BiCMOS process.

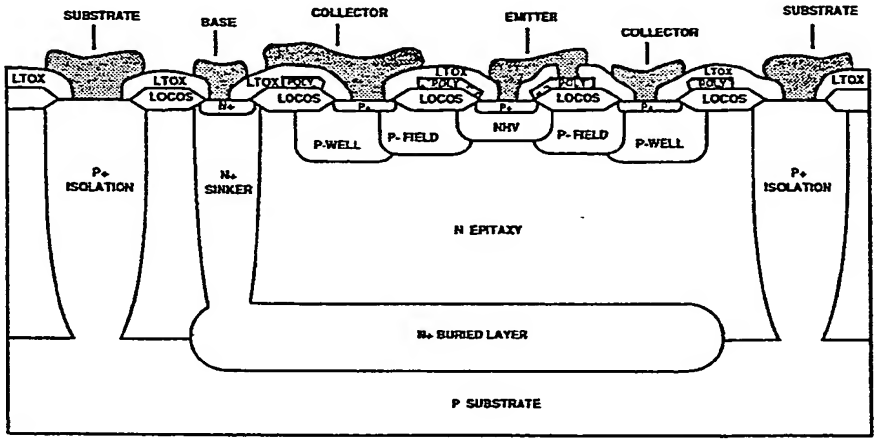


Fig. 2 Improved lateral PNP device cross-section.

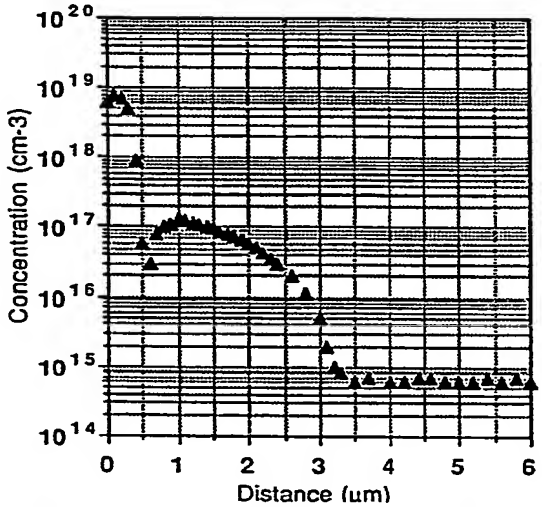
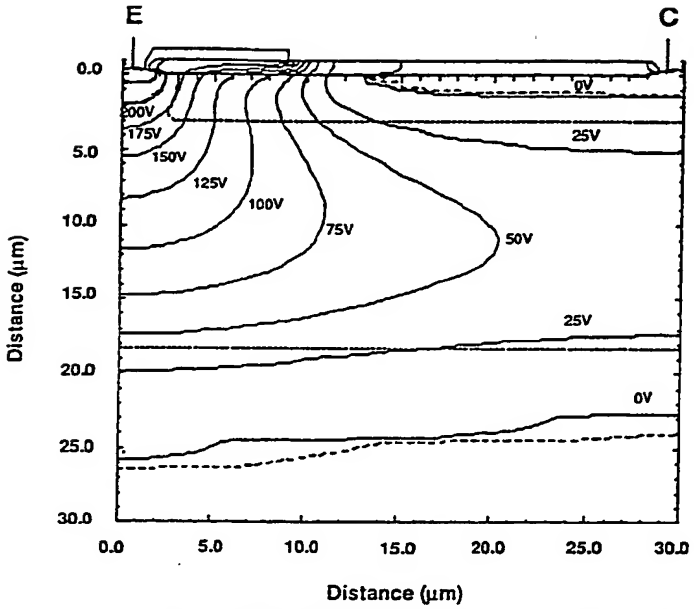


Fig. 3 Vertical impurity profile through emitter and base of improved lateral PNP, measured with spreading resistance probe.

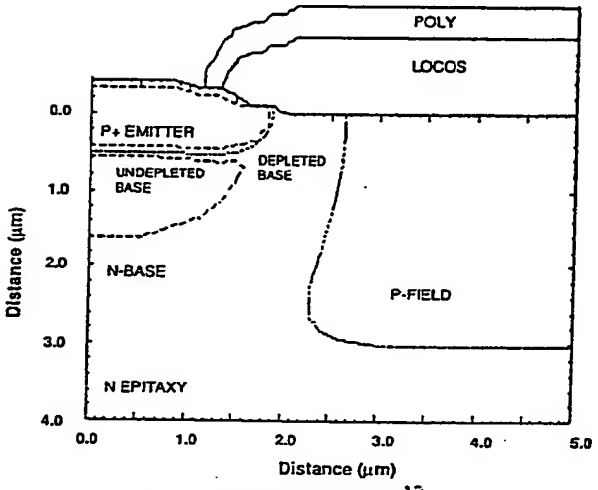


CARRIER IONIZATION INFORMATION

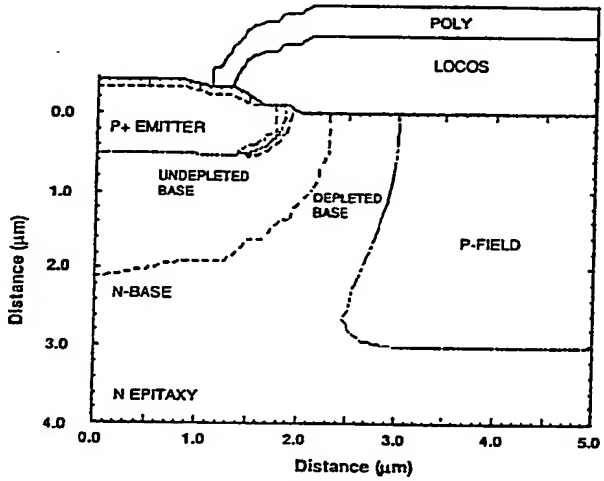
NAME	ELECTRON IONIZATION	PEAK FIELD (V/CM)	X LOCATION (MICRONS)	Y LOCATION (MICRONS)
NEPI	0.6182	2.7668E+05	2.1200	2.030
PFLD	1.0480	4.6484E+05	8.9570	9.9998E-03
SOURCE	1.010	3.5590E+05	2.902	0.8204
DRAIN	0.1779	2.0636E+05	0.9384	2.640
SUBSTRATE	0.1780	2.0636E+00	0.9389	2.640

NAME	HOLE IONIZATION	PEAK FIELD (V/CM)	X LOCATION (MICRONS)	Y LOCATION (MICRONS)
NEPI	0.1178	2.7668E+05	2.120	2.030
PFLD	1.288	4.6484E+05	8.957	9.9998E-03
SOURCE	1.066	3.5009E+05	2.833	0.5255
DRAIN	7.0270E-03	2.0636E+05	0.9384	2.640
SUBSTRATE	7.0352E-03	2.0636E+05	0.9389	2.640

Fig. 4 Typical CANDE 2-D simulation showing equipotential contours in 25 volt increments, for an emitter to collector bias of 200 volts, with tabulation of ionization coefficients and peak electric field values.



(a) N-base(peak) = 2.0×10^{17} cm^{-3}



(b) N-base(peak) = 1.0×10^{18} cm^{-3}

Fig. 5 CANDE graphical output showing the elimination of base punchthrough.

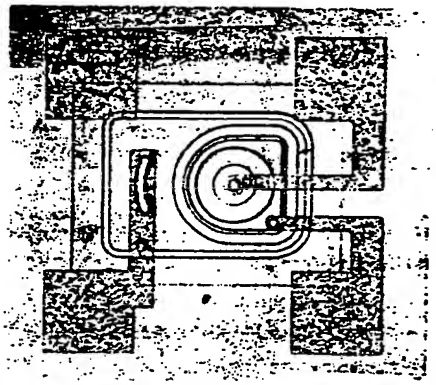


Fig. 6 Die photo of the improved lateral PNP.

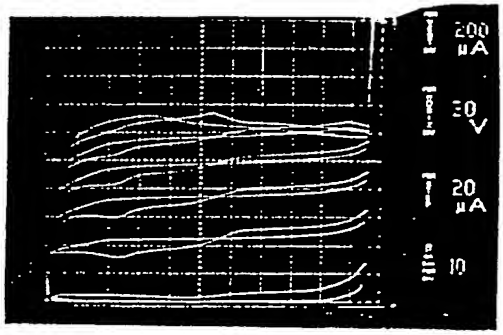


Fig. 7 I_C vs. V_{CE} characteristics of the improved lateral PNP demonstrating a BV_{CEO} of approximately 200 volts.

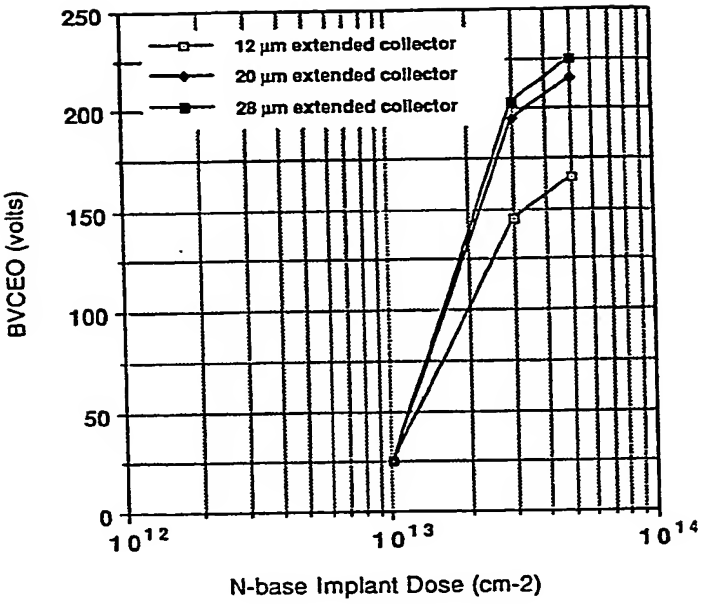
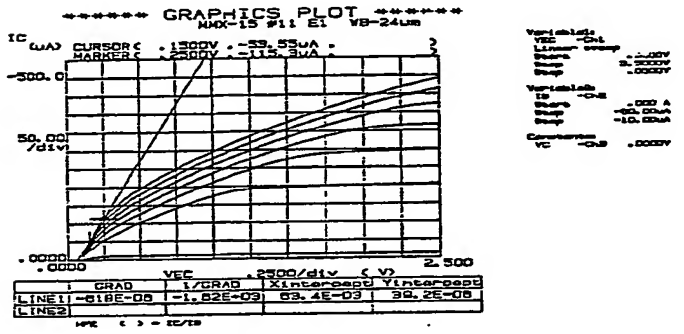
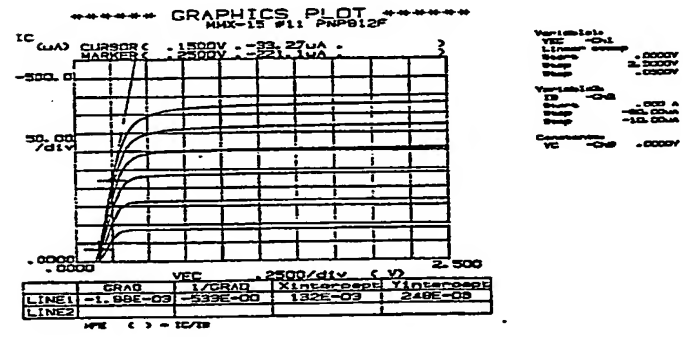


Fig. 8 Measured BV_{CEO} vs. N-base implant dose.



(a) conventional lateral PNP



(b) improved lateral PNP

Fig. 9 Comparison of I_C vs. V_{CE} in the saturation region for the (a) conventional vs. the (b) improved lateral PNP.

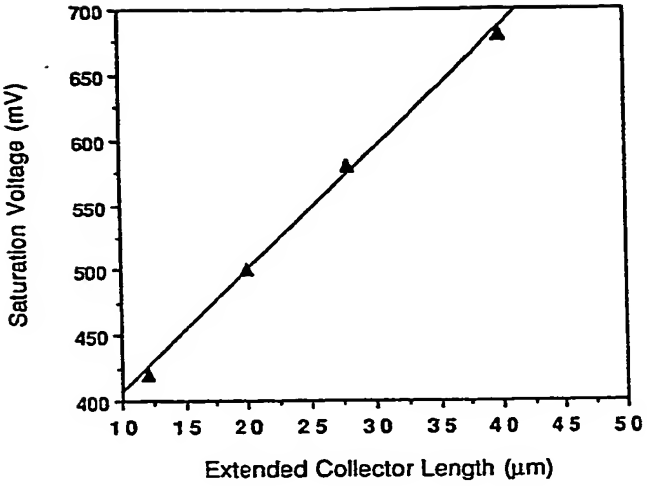
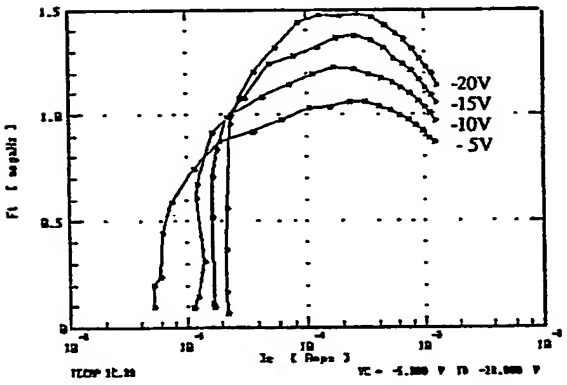
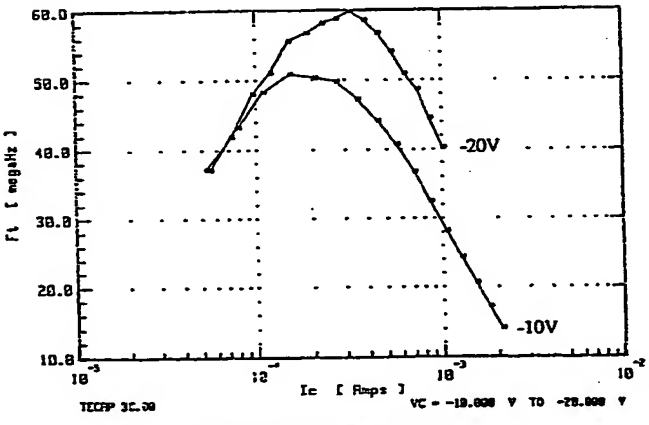


Fig. 10 Measured saturation voltage vs. drawn extended collector length.



(a) conventional lateral PNP



(b) improved lateral PNP

Fig. 11 Unity-gain frequency (f_T) vs. collector current (I_C) derived from s-parameter extraction for the (a) conventional lateral PNP vs. the (b) improved lateral PNP.